

The ModularEEG Design

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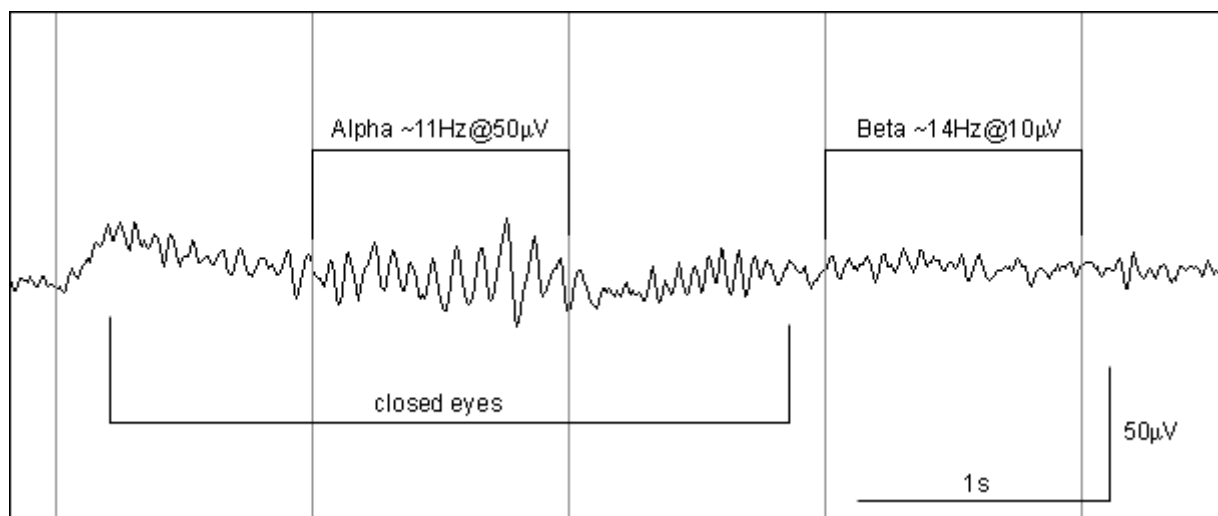
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1. Introduction

The hardware-side of the OpenEEG project (<http://openeeg.st.net>) is about building a cheap EEG device. Since the market for these things is rather small, professional units are too expensive for most people to just buy and experiment with. The ModularEEG is a 2-6 Channel Biosignal Amplifier that has been designed by Jörg Hansmann in 2001 and has been built by many EEG-hobbyists, artists and some academic Institutes that work in this area. Though no exact calculation has been made, it is estimated that a two-channel ModularEEG costs about 200 USD to make.



Example EEG graph, recorded with ModularEEG (courtesy of Nelo).

This wave was captured on a ModularEEG v0.06, with home-made saline-sponge electrodes placed at C3 and P3. C3 and P3 are two points on the head, defined by the 10-20 system for electrode placement. Any search engine will help you find more on that.

To the right, you see beta activity, which is what a brain emits when it is awake and alert. When the eyes are closed, alpha waves dominate the EEG. This happens because P3 is located fairly close to the visual cortex, which emits alpha waves when it is idle.

2. Hardware description

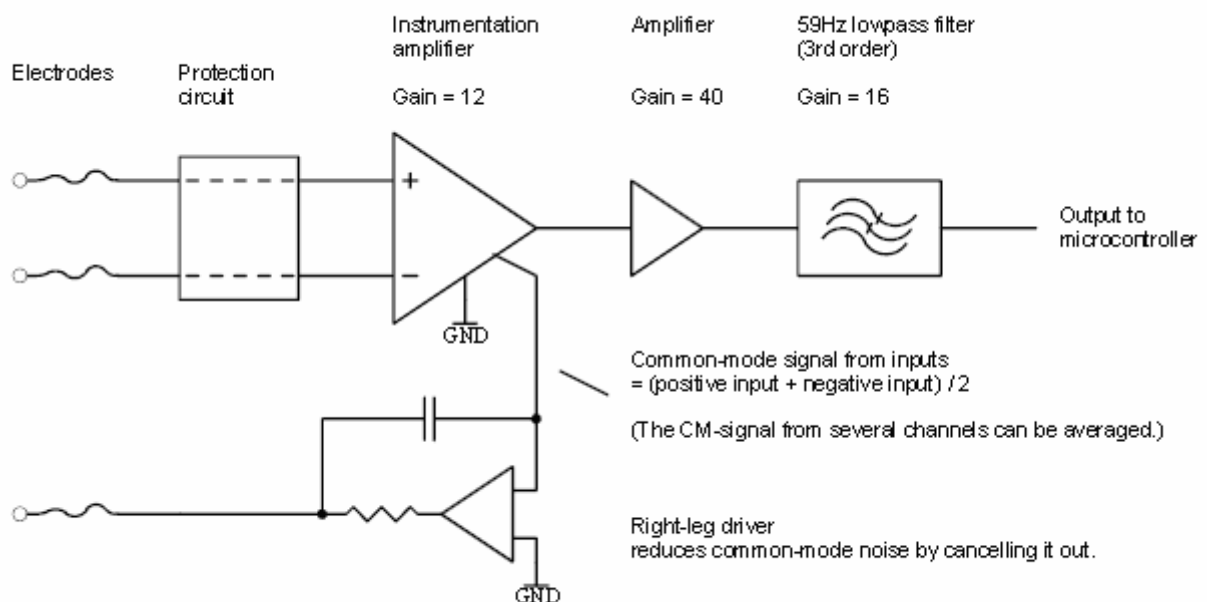
2.1 Overview

An EEG signal is usually acquired through silver-chloride covered electrodes, though sometimes other materials like pure silver, tin, steel or gold are used. The signal amplitude is only a few microvolt and needs to be amplified several thousand times before it can be captured. Because it is faint, the signal can very easily drown in noise, particularly 50/60Hz hum from the mains which is transmitted capacitively (i.e. by an electric field) from the wiring in your house.

To handle this, the signal is first amplified by a high quality instrumentation amplifier, which measures the voltage difference between two locations on the scalp. In the example in the previous section, we used C3 and P3. This ensures that a large percentage of the mains hum never enters the system, because the level of the mains hum on those two locations is essentially the same.

Afterwards the signal strength is increased further by normal amplifiers, and passed through a low-pass filter which minimizes distortion caused by so-called aliasing that may occur when the signal is converted to digital samples.

Below is the block diagram of one EEG amplifier channel, and the Right-leg driver (DRL-circuit).



Simplified block diagram of the ModularEEG amplifier

Some parts are not included here. The schematic gives you all the details if you are interested.

The EEG signal is picked up by the two topmost electrodes and passed through the protection circuit. It serves two purposes: First, it protects the circuitry from electrostatic discharge (ESD) and second it protects the user from failing circuitry. In theory at least.

Leaving the protection circuit, the signal enters the instrumentation amplifier where it is amplified 12 times. After that, the signal is amplified about 40 times in a second amplifier stage. You can't see it in the diagram, but there is a reason for splitting the amplification into two steps like this. Between the two stages there is a high-pass filter which removes DC-voltage offsets.

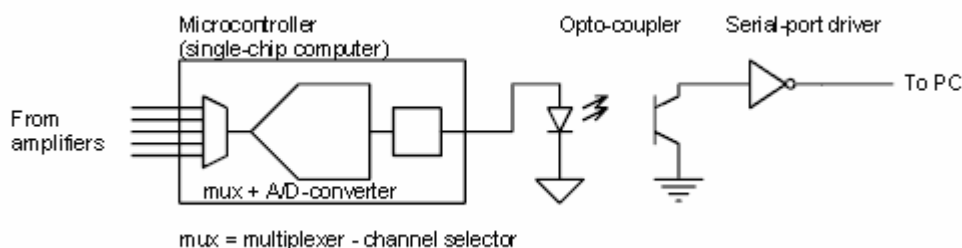
Some electrode materials, such as gold or steel, are polarizable. This means that electric charge can accumulate on the surface of the electrode, building up a relatively large DC-voltage, sometimes several hundred millivolts if you are unlucky. In theory, you would amplify a 200mV signal 480 and get a 96 volt output. In reality, the circuitry can handle about 2.5V so the output signal would be stuck at a maximally high or low level, usually $\pm 2.5V$ and not contain any EEG. The highpass filter tries to solve this problem.

Finally, the signal is amplified 16 times more and lowpass filtered. The filtering is done to prevent aliasing effects later on, when the signal is digitized.

Below the signal amplifiers, and the filter, sits a third amplifier pointing the other way, seemingly sending a signal to the user. This is the right-leg driver. It is named like this for historical reasons. The driver is, and was, previously only used by ECG meters, which measures the electrical activity in the heart. During ECG sessions, the driver (also abbreviated DRL, for Driven Right Leg) is attached to the right leg, as far away from the heart as possible.

The purpose of the DRL is to reduce common-mode signals such as 50/60Hz mains hum, by cancelling them out. It replaces a ground electrode which older EEG designs use, and can attenuate mains hum up to 100 times more than the instrumentation amplifier can do by itself.

After the filtering, the signal is ready for acquisition by the analog-to-digital converter which in our case is located inside a microcontroller. The microcontroller sends the digitized EEG to a PC via a standard serial cable. To protect the user from electrical faults, the EEG device is electrically isolated from the PC and external power sources. The block diagram below shows this.



Simplified block diagram of the ModularEEG microcontroller, optocoupler and RS232 interface.

Please note that the ModularEEG is not tested according to medical safety standards, and should be considered experimental at best.

2.2 Technical specifications

General specification

| | |
|---|--------------------------|
| Number of channels | 2 - 6 (only 2 tested) |
| Resolution | four 10 bits, two 8 bits |
| Input Voltage Resolution | 0.5 μ V |
| Input Voltage Full Scale | +/-256 μ V |
| Wideband noise | \sim 1 μ Vp-p |
| Supply Current (5V or 9 - 12V supply) | 70 mA (2 channels) |
| Isolation voltage (<i>note 2, 3</i>) | 2500V (1 minute) |
| Continuous isolation voltage (<i>note 2, 3</i>) | 480V |

1. On the ATmega8 microcontroller, channels 5 and 6 are only 8 bit due to noise problems. These channels can not be used for EEG without increasing the EEG-amplifier gain four times.
2. The DCDC converter and optocoupler are certified to withstand 3000Vrms and 2500Vrms respectively, for one minute. The guaranteed working voltage under periods longer than one minute is 1100Vrms and 480Vrms respectively.
3. The ModularEEG is not IEC60601-1 certified. It will probably not handle lightning strikes and other extreme electrical conditions. Use with caution.

Supply Current

| | |
|---|--|
| Digital board | 52 mA |
| Digital board + serial cable connected | 56 mA |
| Total current (including 2 channel amp) | 73 mA |
| Estimated total for 4 channel setup | 77 mA |
| DC/DC converter efficiency | \sim 78% (\Rightarrow 15mA, 2 ch) |

EEG Amplifier specification

| | |
|----------------------------|--|
| Gain | 7812.5 (nominally) |
| Offset handling capability | TBD > 200 mVdc |
| Low frequency CMRR | TBD > 100 dB (?) |
| Highpass filter | 2nd order, f_c = 0.4Hz |
| Anti-aliasing filter | See filter document. |
| Extra features | 250 μ V(+/-10%) test signal. DRL circuit - adds > 40dB CMRR at 50/60Hz. |

AD-converter specification (AT90S4433)

| | |
|---|----------------------------|
| Number of channels | 6 |
| Resolution | 10 bits |
| Effective number of bits (<i>note 1, 3</i>) | 9.1 bits (< 100Hz) |
| Signal to Noise Ratio (<i>note 1, 3</i>) | 58.7dB (max possible 60dB) |
| Integral Nonlinearity (<i>note 2</i>) | +/- 0.5 LSB (typ) |
| Differential Nonlinearity (<i>note 2</i>) | +/- 0.5 LSB (typ) |
| Offset Error (<i>note 2</i>) | 1 LSB (typ) |
| Absolute Accuracy (ADC clock = 200kHz) | 1 LSB (typ), 2 LSB max |
| Gain error (Voltage reference error) | 1% (typ), 2.25% max |

Notes

1. Dynamic characteristics are taken from *Holcher, R. et. al., The Test of AD Converters Embedded on Two Microcontrollers, Measurement Science Review (Journal of the Institute of **Measurement Science**, Slovak Academy of Sciences, <http://www.measurement.sk/>), Volume 1 Number 1 2001.*
<http://www.measurement.sk/PAPERS/Holcer.pdf>
2. INL, DNL, offset error and absolute accuracy numbers are taken from the manufacturers data sheet. The article in note 1 specifies a higher INL: 1.4 LSB max (absolute value, not +/- 1.4 LSB). All values assume ADC clock < 200kHz. Yeah, these numbers could be better.
3. The article in note 1 discusses the AT90S8535 microcontroller. This is a bigger microcontroller in the same family as AT90S4433, so chances are they have very similar cores. The measurements were done at a higher sample rate ($f_s = 4800\text{Hz}$) and with $V_{ref} = 2.5\text{V}$ which may degrade the results slightly compared to the $f_s = 256\text{Hz}$ and $V_{ref} = 4.0\text{V}$ used in the ModularEEG.

2.3 Detailed description

In the following sections, we will work our way from the EEG inputs to the serial port output. Note that while describing the analog board, the part numbers used in channel 2 are omitted for clarity. Important: To make sense of the following sections, you will need the schematics.

Protection circuit

The first stop after entering the analog board via the EEG connectors, is the protection circuit.

At the front sits three capacitors, C210, C206 and C207 that are supposed to suppress radio-frequency signals entering the system via the electrode cable. They are followed by a network of transistors (Q202, Q204, Q206 Q208) and some resistors (R203, R204 and R209 to R212).

The transistors are not actually used as such, instead they act as clamping diodes.

When the voltage over one of these "diodes" exceeds about 0.2 volts, they start to conduct current. Below that level, they are basically open circuits, only conducting a few picoamperes. If the voltage reaches about 0.7 volts, they begin to conduct in earnest. With the help of the resistors they prevent the voltage from ever going above 0.7 volts. They also limit the current going through a user, in case of short circuit between a power rail and an amplifier input pin.

Amplifiers and filters

Behind the protection circuit sits the instrumentation amplifier IC203. It not only amplifies the EEG but lowers the impedance, making it less sensitive to noise. The gain is set by the R216 and R217 according to $G = 1 + 50 \text{ k}\Omega / R_g$, where $R_g = R216 + R217$. In the junction between R216 and R217 it is possible to measure the common mode voltage. IC204A does this, and then passes the signal on to the DRL

After the instrumentation amplifier, there is a highpass filter made from C221 and R226, which is designed to remove DC offsets. Its cutoff frequency is about 0.16Hz.

A standard, non-inverting amplifier circuit follows the high pass filter. The gain is set as $G = (R_a + R_b) / R_a$, where $R_a = P203 + R222 = 1\text{k}\Omega$ to $21\text{k}\Omega$, and $R_b = R225 = 100\text{k}\Omega$, allowing the gain to be set to 6 to 100.

Finally, there is a second highpass filter stage, identical to the first, and a 3rd order lowpass filter which also amplifies the signal another 16 times, with the operational amplifier IC206B at its center. The filter is described in detail in Appendix A.

Note that only two poles of the filter are located on the amplifier board. If you look at the schematic for the digital board, you will find a set of RC-links made up of $7.5\text{k}\Omega$ resistors and 220nF capacitors that form the third pole. They are placed quite close to the microcontroller in order to reduce interference that may have been picked up in the board-to-board cable.

Right-leg Driver

As was mentioned in the previous section, the common-mode signal is tapped at the junction of R216 and R217 and then passed through IC204A. The other channel is handled similarly.

The rest is TODO...

RS232 Interface

The serial interface has three parts: A classic MAX232 (IC106) that converts the RS232 voltage levels, $\pm 12\text{V}$ usually, to TTL levels (0 and 5 volts) and vice versa. Two optocouplers (IC103 and IC104) electrically isolates the MAX232 from the rest of the board, for safety reasons. For someone who has used optocouplers before, the circuitry (the resistors) around the optocouplers may look a bit different. It allows higher transmission bitrates by reducing the voltage swing needed to change from zero to one or one to zero.

The original optocoupler design is found in the German book "Mit dem PIC-Controller erfolgreich arbeiten." by Anne and Manfred König, ISBN: 3827251680.

It is important to note that individual optocouplers have large differences in current-transfer-ratio (CTR). The CTR parameter specifies how much of the current powering the transmitter-LED that is "transferred" to the receiver-phototransistor, and affects the performance of the circuit. If you are unlucky you may have to change the 470 ohm resistors to get signals across. Ask for help on the mailing list if you have problems sending or receiving serial data.

Microcontroller

The microcontroller is an AT90S4433 (soon obsolete) or ATmega8 manufactured by Atmel. It was selected for several reasons:

- It is quite fast. Most instructions only take one clock cycle to execute.
- It has a built in 6-channel 10-bit AD-converter making it possible to measure 6 EEG signals at the same time, with three amplifier boards. In the ATmega8, the last two channels are only 8-bit, which is not suitable for EEG, but should still work ok with ECG for example.
- It has a PWM-output. In the ModularEEG it is used to generate a 14Hz square-wave signal. The signal is fed to the analog board where the amplitude is divided down to about 250uV, suitable for testing and trimming the EEG amplifiers.
- It has a full-duplex serial port.
- Programming is very easy and does not require an expensive programmer.

In other words, it does everything that is needed.

The discrete parts to the left of the microcontroller are used for several things, but most of them are dedicated to creating a 4.0V DC signal for the AD-converter.

The voltage reference (IC101) sets the voltage at its cathode by shunting the right amount of current through itself, causing a controlled voltage drop over R107. R107 = 470 ohms limits the current to about 2 mA, but the exact amount is determined by the voltage on the R input on the reference.

R102 and R103 forms a voltage divider and a feedback path for the reference so when the cathode voltage is 4.0V, the R input sees 2.5V which is the set point for this reference. If the cathode voltage is disturbed by a change in the supply voltage, the reference will change the shunting current accordingly, so that it maintains 2.5V on the R input.

Looking at the parts to the left of R102 and R103, the 10uF capacitor is used as a power reservoir, much the same way as any of the decoupling capacitors you will find all over the board. The diode D101 is used to ensure the reference voltage never exceeds the supply voltage during power off.

R101 and R105 divides the 4.0V in two, creating an unbuffered 2.0 volt reference for the VGND net. After that it is buffered on the analog board. A buffer is simply an amplifier with gain = 1 commonly used to provide drive capability. Drive capability is

the ability to force a signal to change, or to keep it at a desired level, by sinking or sourcing current into the wire.

In this case, drive is not that important, because the signal is constant. It would have been nice to have a buffer nearby to help fend off noise, but unfortunately there is no room for it. However it appears to work anyway, with a (not-so-wideband) buffer amplifier (IC201A) on the analog board. Finally, R111 and C108 (100 ohms + 10nF) provides extra HF-rejection for the analog power input to the microcontroller.

Power System

There are two ways to power the ModularEEG. The recommended way is by a 9V or 12V battery, but it is possible to use an external 5V supply. Looking in the top right corner of the digital schematic, we see that a power source can be connected to the pads marked PWR and GND1 respectively. If we are using a 9 or 12V battery, D103 prevents damage from reversed polarity. D104 is not used in this case and need not be mounted. After the diode sits a standard 7805 voltage regulator and a few capacitors that act as current reservoirs.

The output from the 7805 powers two parts of the circuit; the RS232 interface described below, and a DCDC converter. The DCDC converter has one very important job; it transmits electricity across the isolation barrier, powering the rest of the ModularEEG while protecting the user from overvoltages. It can withstand continuous voltages of up to 1100 volts and spikes up to 3000 volts across its input and output.

Following the DCDC converter sits two filters, made up by the inductors L101 and L102 and three capacitors each. We need more than one capacitor, because real-world caps are far from ideal: they only work well within a limited frequency band. The 10 nF capacitors handle the highest frequency components while the 47 uF capacitors handle the lowest frequency components.

The purpose of these filters is to reduce the switching noise from the DCDC converter. The power going to the microcontroller's digital part is filtered once, and the power going to the analog part and amplifiers is filtered twice.

The amplifiers on the analog board needs a dual power supply, but the power supply only provides a single voltage. To solve this problem, a "virtual" ground point is created by feeding a 2V signal to an operational amplifier, IC201A on the analog board. IC201A then "drives" the virtual ground, named VGND. More information on how this 2V VGND signal is created is found in the microcontroller section, below.

In short, what is used as GND on the digital board is renamed AGND and used as the negative power rail on the analog board. $VGND = AGND + 2 \text{ volts}$ acts as a virtual ground point for the amplifiers.

On the analog board, IC201A is decoupled by a large 47uF tantalum capacitor, C201. If you are experienced with analog electronics, this may seem a bit counterintuitive and counterproductive, but in this case a large capacitive load helps stabilizing the output.

C201 is a bit different from other capacitors. All capacitors have some series resistance (ESR), and in this case the value is important. An ESR of roughly 1 ohm helps minimize ringing in the VGND plane, caused by sudden and rapid changes in the amount of current drawn from the power supply.

Now, let us go over the power networks again.

Starting on the digital board, in the unisolated section, where power comes in and RS232 signals go out, we have

PWR = incoming unisolated power

+5V/1 = Unisolated, regulated 5V

GND1 = Unisolated ground

The DCDC converter bridges the gap between unisolated and isolated and we have

+5V/3 = Isolated 5V for the digital parts

+5V/2 = Isolated and filtered 5V for the analog parts, including the amplifiers.

GND = Digital ground.

Finally, on the analog board we have

+5V/2 = Analog power supply

VGND = Virtual ground, +2V referred to AGND

AGND = GND on the digital board

System Firmware

Currently, there are two standard transmission protocols to send the eeg-data from ModularEEG to the host computer, which are described in the following:

ModularEEG Packet Format Version 2 (P2)

The beginning of a Packet is indicated by the two sync-bytes 'A5 5A', followed by the Version Number, the Packet - Counter and the Values for 6 Channels (16bit integers, -> 12 bytes). The last byte represents the status of the 4 pushbuttons of the modularEEG in the lower nibble. This makes a total of 17 bytes per packet:

- 1: A5 // first sync-byte
- 2: 5A // second sync-byte
- 3: version-Number
- 4: Packetcount
- 5: chn1-hibyte
- 6: chn1-lowbyte
- 7: chn2-hibyte
- 8: chn2-lowbyte
- 9: chn3-hibyte
- 10: chn3-lowbyte
- 11: chn4-hibyte
- 12: chn4-lowbyte
- 13: chn5-hibyte
- 14: chn5-lowbyte
- 15: chn6-hibyte
- 16: chn6-lowbyte
- 17: buttonstate

ModularEEG Packet Format Version 3 (P3)

One packet can have zero, two, four or six channels (or more).
The default is a 6-channel packet, shown below.

| | |
|-----------|---------------------|
| 0pppppppx | packet header |
| 0xxxxxxx | |
| 0aaaaaaaa | channel 0 LSB |
| 0bbbbbbbb | channel 1 LSB |
| 0aaa-bbb | channel 0 and 1 MSB |
| 0ccccccc | channel 2 LSB |
| 0ddddddd | channel 3 LSB |
| 0ccc-ddd | channel 2 and 3 MSB |
| 0eeeeeee | channel 4 LSB |
| 0fffffff | channel 5 LSB |
| 1eee-fff | channel 4 and 5 MSB |

Key:

1 and 0 = sync bits. Note that the '1' sync bit is in the last byte of the packet, regardless of how many channels are in the packet.

p = 6-bit packet counter

x = auxillary channel byte

a - f = 10-bit samples from ADC channels 0 - 5

- = unused, must be zero

There are 8 auxillary channels that are transmitted in sequence.
The 3 least significant bits of the packet counter determine what channel is transmitted in the current packet.

Aux Channel Allocations:

0: Zero-terminated ID-string (ASCII encoded).

1:

2:

3:

4: Port D status bits

5:

6:

7:

The ID-string is currently "mEEGv1.0".

A. Filter specifications

Note: A capacitor in the filter (C7 in the schematic below) has been changed to 1nF. That means that these specs are out of date and that some of the numbers, and all of the graphs in the sections below are inaccurate for ModularEEG v1.1 or later.

The change was made to remove ringing (higher-frequency oscillation) that was observed when the amplifier was fed with the 14Hz square wave test signal.

However, this increase in stability comes with a few drawbacks. First of all, the filter is now less efficient at preventing aliasing. (To be honest, it wasn't very good to begin with.) Second, the "knee" of the frequency response is now much softer, which has an impact on signals in the 10-40Hz range. Attenuation starts at roughly 10Hz and drops off gradually. At 40Hz, signal strength is down 10% (1 dB).

If you want the performance shown below, you can of course use a 10nF capacitor...

TODO: Make new graphs.

A.1 Description

There are three distinct parts in the anti-aliasing filter in the ModularEEG

1. An amplification-only stage with a nominal gain of 40. Using a 10kOhm trimpotentiometer, the gain can be set to anything between 10 and 100.
2. Two simple highpass filter stages.
3. A lowpass filter stage with $f_c = 59$ Hz that also provides a gain of 16.

Parts 1 and 2 are not described further, though their effect on the output is visible in the graphs below. Total gain is 640, or roughly 56dB.

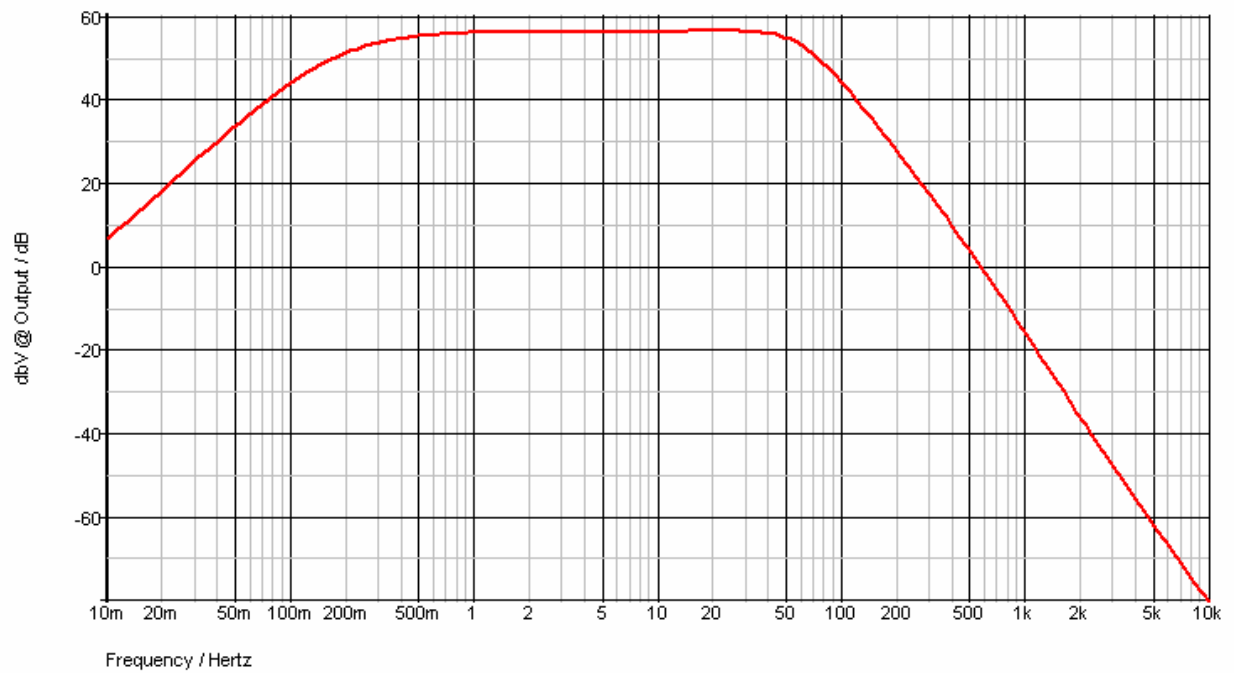
The third part, is what might be described as a "Besselworth" filter (not a standard name) as it is modelled to be a blend of a Butterworth and a Bessel filter; The group delay is flatter than that of a Butterworth filter, but not absolutely flat as that of a Bessel filter. The "knee" on the boundary between the pass and transition bands is more rounded than that of a Butterworthfilter, yet sharper than that of a Bessel filter.

Counting the capacitors in the schematic, one might be led to believe that this is a 4th order filter. Strictly speaking, it is not. A 1st order filter has a rolloff of 6dB per octave, a 2nd order filter has 12dB per octave, a 3rd order filter - 18dB per octave, etc. This filter has a 19.2dB rolloff per octave, so the order might be described as closer to 3.2.

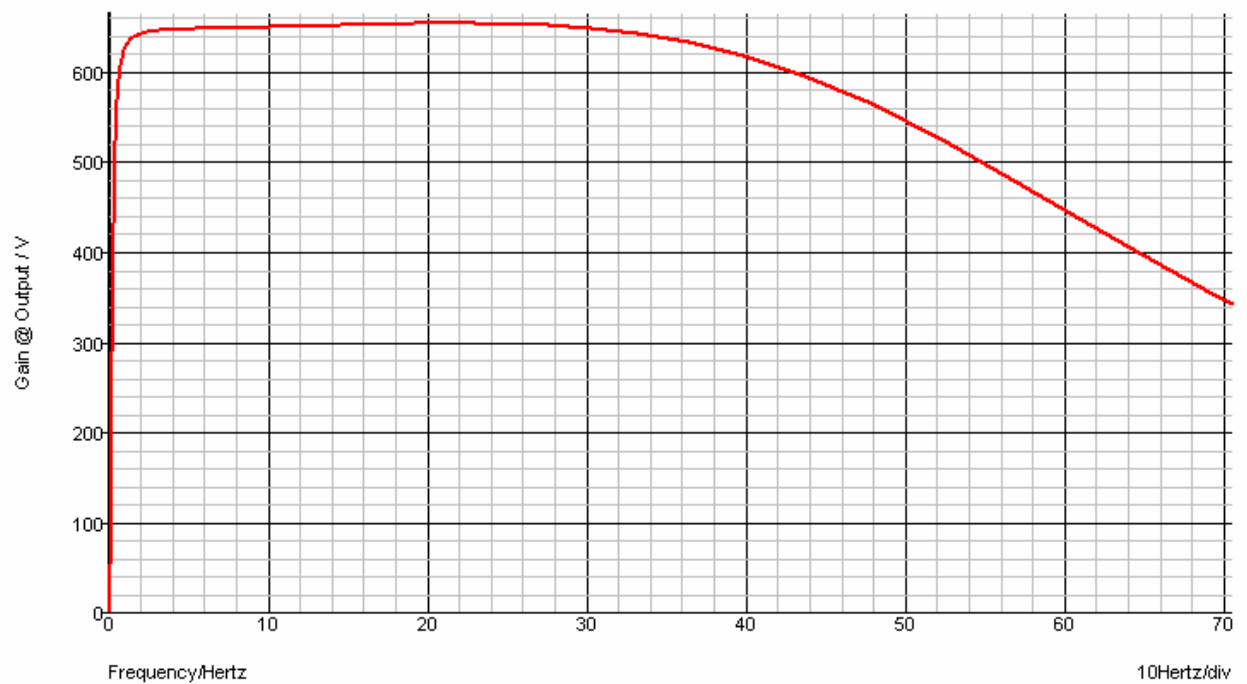
The filter is good enough to prevent all aliasing artifacts in a 10-bit AD-converter with 9 effective number of bits, if the sample rate is approximately 1.5kHz or higher. Since this rate is too high to be usable with more than two channels on a standard serial port, a sample rate of 768 Hz is sufficient if aliasing is permitted above 50 Hz.

However, because the signal we are trying to measure (EEG) is naturally filtered by the skull, it is quite possible that a lower sample rate, for example 256 Hz or 512 Hz is sufficient for most purposes.

A.2 Gain

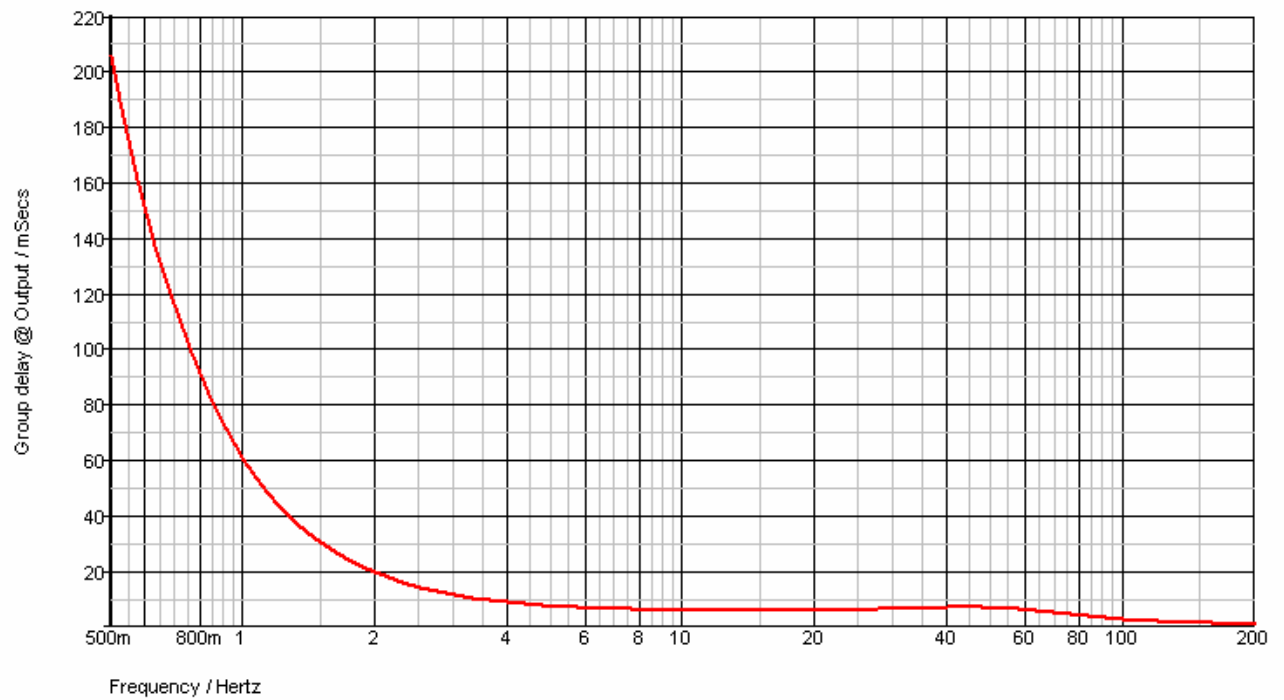


Filter gain - dB scale

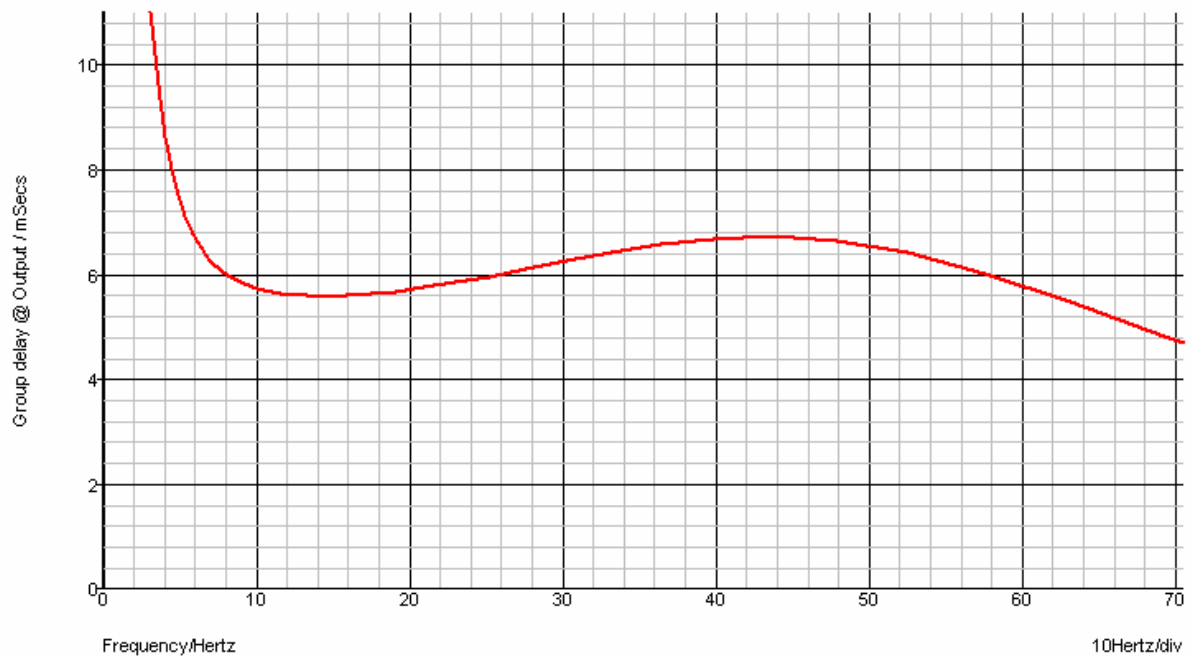


Filter gain - linear scale

A.3 Group Delay

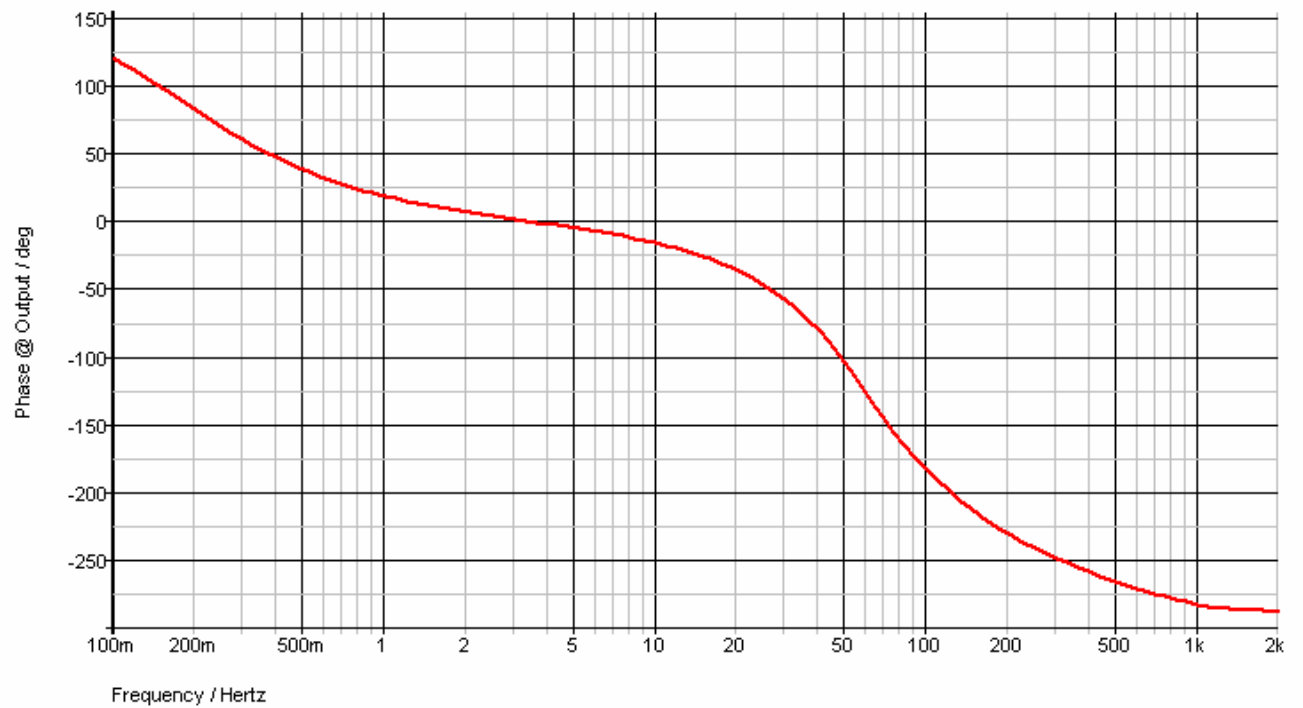


Group delay - logarithmic scale

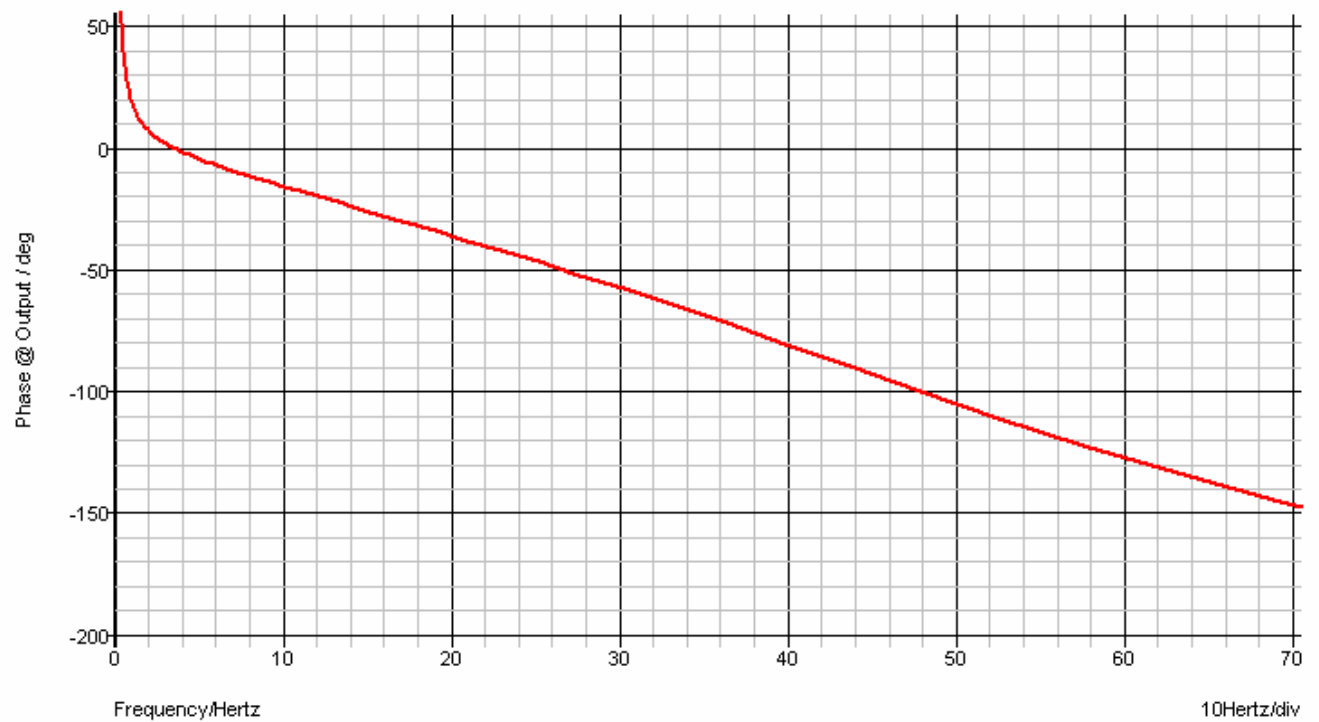


Group delay - linear scale

A.4 Phase

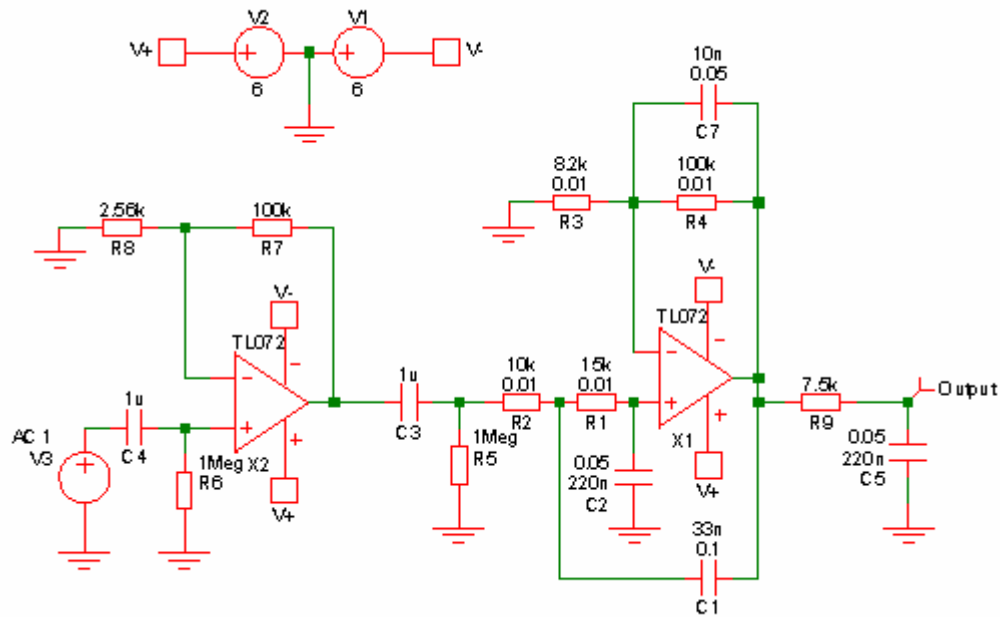


Phase response - logarithmic scale



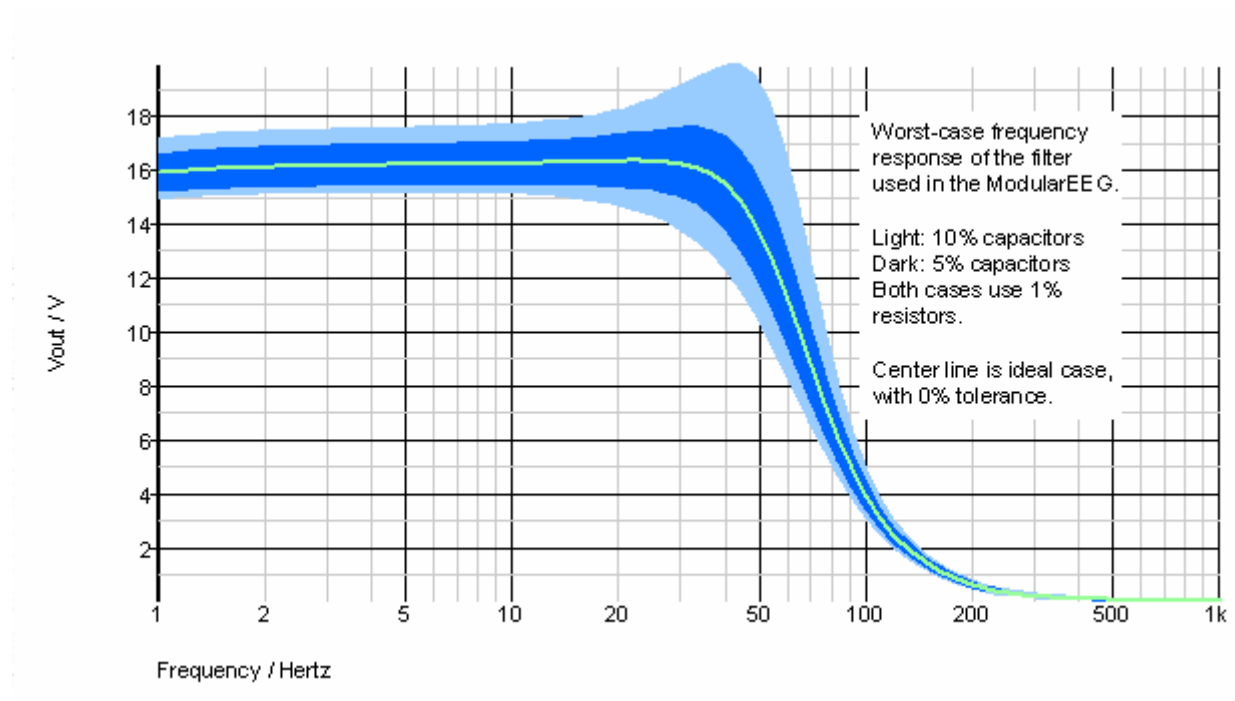
Phase response - linear scale

A.5 Schematic



SPICE schematic

A.6 Component tolerances



The effect of different capacitor tolerances on the frequency response